MINIMIZING THE ELECTRICAL LOSSES ON THE FRONT SIDE: DEVELOPMENT OF A SELECTIVE EMITTER PROCESS FROM A SINGLE DIFFUSION

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ABSTRACT

In this paper we present latest results in the development of a process for the fabrication of a selective emitter structure on mono- and multicrystalline silicon solar cells. The process is based on an approach that was first introduced by Zerga et al. [1]. We have chosen a wet chemical route for an emitter etch back where the areas of the wafer that are intended for emitter metallization are shielded from etching by a screen printable etch barrier. The etch barrier is later removed by wet chemical etching. The process has yielded a gain in open circuit voltage of more than 1% and a gain in short circuit current of more than 2%. The overall efficiency gain was more than 0.3%$_{abs}$ due to slightly lower fill factor of the cells.

INTRODUCTION

The electrical losses in the emitter of standard screen printed mono- and multicrystalline silicon solar cells have become one of the dominant factors limiting the cell performance of today`s industrially produced cells. The tradeoff between a low and homogeneous specific contact resistance of the screen printed silver metallization on one side and a reduction of the saturation current in the emitter and at the surface on the other has led to the widespread use of an emitter doping profile that is characterized by a very high surface concentration, a sheet resistance of 45-60 Ω/Sq and a junction depth of ≈ 500 nm.

It can been shown that a decrease of the surface concentration and a reduction of the thickness of the dead layer has the potential of significantly reducing the losses that stem from Auger-recombination within the very highly doped regions and from SRH-recombination occurring at the surface due to a mediocre surface passivation.

We have developed a new etching technique that permits a controlled reduction of the emitter surface concentration within a relatively wide process window. The process is fully compatible with and can be easily integrated into existing large scale production lines. In our laboratories it has led to a significant increase of the solar cell performance.

CELL PROCESSING

The cell fabrication process is suitable for both mono- and multicrystalline substrates. The processing sequence is shown in Fig. 1.

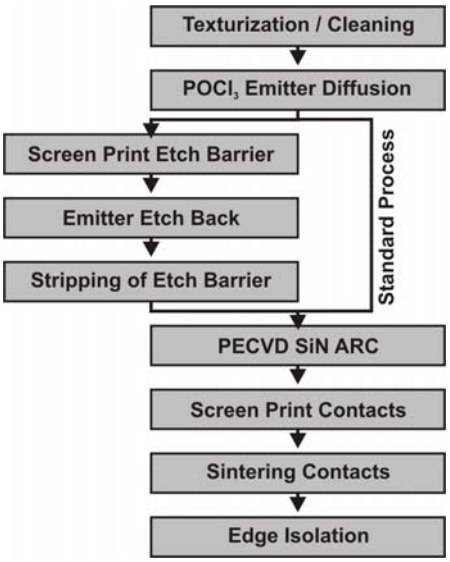

Fig. 1: Processing sequence of solar cells with selective emitter (left) and standard cells (right).

After random pyramid texturization - in future experiments an acidic texturization will be used for multicrystalline substrates - and cleaning the wafers underwent a 50 Ω/Sq $POCl_3$-diffusion. Then an etch barrier was screen printed onto the wafer and subsequently cured. To decrease the surface concentration of the emitter dopant the wafers were submerged in an acidic etch bath. After the etch back the barrier was removed by wet chemical etching and a PECVD SiN_x antireflection coating was deposited on the front side. Afterwards the emitter and rear side metallization were screen printed and sintered. Fig. 2 shows a schematic of the cell design.

DEVELOPMENT OF ETCH SOLUTION

In order to reach an optimal cell performance it is essential to achieve a very homogeneous etch back of the emitter to avoid a locally strong increase of the series resistance of the cell.

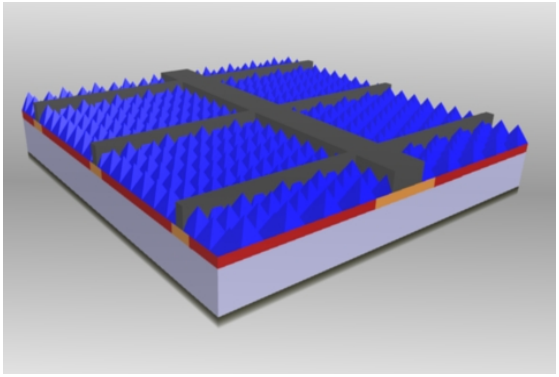

Fig. 2: Layout of a screen printed silicon solar cell with a selective emitter design. The heavily doped regions are located underneath the emitter metallization whereas the remaining areas are more lightly doped.

We have tried several etch back solutions to achieve an optimal homogeneity. We have found that especially for multicrystalline substrates an aqueous solution of KOH and isopropanol does not provide a sufficient homogeneity (Fig. 3).

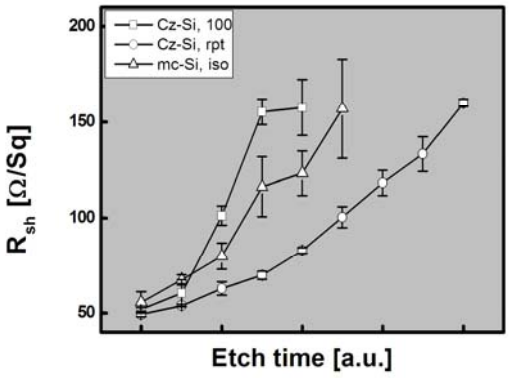

Fig. 3: Temporal development of the sheet resistance and its standard deviation of a phosphorous doped emitter in an alkaline etch solution of KOH and isopropanol at a temperature of 50°C for three different substrates (100-oriented, random pyramid textured and multicrystalline).

In contrast an acidic etching solution from $HF/HNO_3/H_2O$ provides a sufficient homogeneity if adjusted appropriately. Without the need for cooling we have found that this solution allows for a much better process control than its alkaline counterpart. To optimize the etching process for batch or inline machinery it is possible to adjust the etching rate by means of concentration of the chemicals as well as the bath temperature.

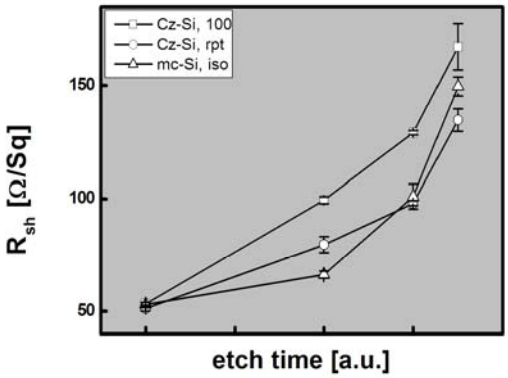

Fig. 4: Results of sheet resistance measurements of a 50 Ω/Sq phosphorus emitter submerged in an acidic etch bath of $HF/HNO_3/H_2O$. The acidic solution achieves a much better etch back homogeneity than the investigated alkaline solution.

To determine the saturation current density of etched back emitters passivated by a low-frequency direct plasma PECVD SiN_x layer QSSPC-measurements of symmetrical samples have been carried out. Starting from an initially more heavily doped emitter (~30 Ω/Sq) the samples were subsequently etched back to 50, 100 and 150 Ω/Sq. It can be seen that an etched back emitter shows a lower saturation current when passivated with a PECVD SiN_x than the typical industrial emitter used at the University of Konstanz, even though both possess the same sheet resistance. The saturation current density of the etched back emitter is about 65 fA/cm² lower than that of the standard emitter doping profile.

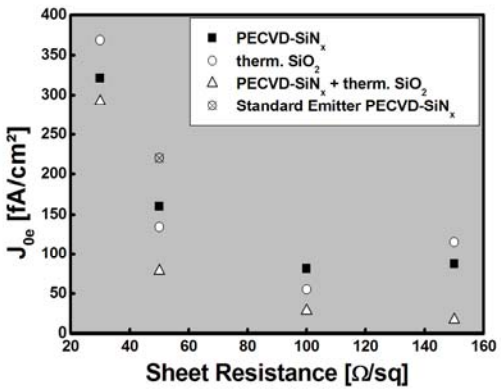

Fig. 4: QSSPC measurements of an etched back and a standard emitter passivated with PECVD SiN_x, thin thermal SiO_2, and a stack of PECVD SiN_x and thermal SiO_2. It can be seen that although having the same sheet resistance the standard emitter displays higher saturation current densities.

CELL RESULTS

Cells were fabricated on 125 mm monocrystalline Czochralski wafers from Deutsche Solar with a specific resistivity of approximately 1.5 Ωcm and a thickness of 240 µm. With the standard screen printed cell fabrication process at the University of Konstanz the wafer material typically yields an average cell efficiency of approximately 17.6%. The etch back process was used to create an emitter sheet resistance of 60, 80 and 100 Ω/Sq. The results from the IV-measurements are shown in Tab. I. The best cell featured an emitter with a sheet resistance of approximately 80 Ω/Sq.

	V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]
best cell	634	36.0	79.4	18.1
avg (23 cells)	631	35.9	78.5	17.9
Standard Process	627	35.7	78.6	17.6

Tab. I: Comparison of the electrical performance of cells with an etched back emitter and cells with a homogeneous emitter structure.

The results shown in Tab. I include a sintering process optimization of the front contacts. This has lead to low fill factors in some cells negatively affecting the average fill factor. Thus, a significant gain in the average efficiency can still be expected.

Spectral response measurements (Fig. 5) show that the internal quantum efficiency (IQE) of an etch back emitter in the short wavelength spectrum is significantly higher than that of a standard industrial emitter. Therefore the increase in J_{sc} can be attributed to the better blue response while the gain in V_{oc} is caused by a lower emitter saturation current.

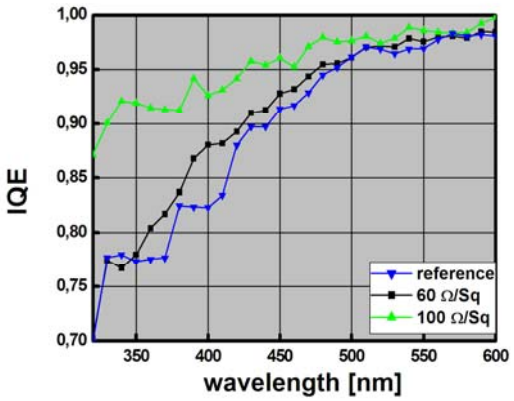

Fig. 5: Calculation of the internal quantum efficiency (IQE) from measurements of the spectral response of cells with emitters etched back to a sheet resistance of 60 and 100 Ω/Sq. It is obvious that the IQE of etched back emitters is significantly higher in the wavelength region from 350 to 500 nm.

ADAPTATION OF FRONT SURFACE PASSIVATION

Measurements of the effective lifetime of samples (p-typ FZ, 0.5 Ωcm) prepared with an etched back emitter have shown that further improvements are possible by an adaptation of the PECVD SiN_x deposition parameters. For a standard emitter a significant increase of the effective lifetime could not be reached by such a variation. Here it seems the sample performance is limited by the emitter itself, For higher sheet resistances the difference between an improved and a standard SiN_x-deposition increases. Apparently, recombination within the emitter is reduced by the etch back process and SiN_x becomes the limiting factor. A change of the deposition parameters in turn yields another significant gain that can probably be translated into an increase of the open circuit voltage (V_{OC}) of the finished cell.

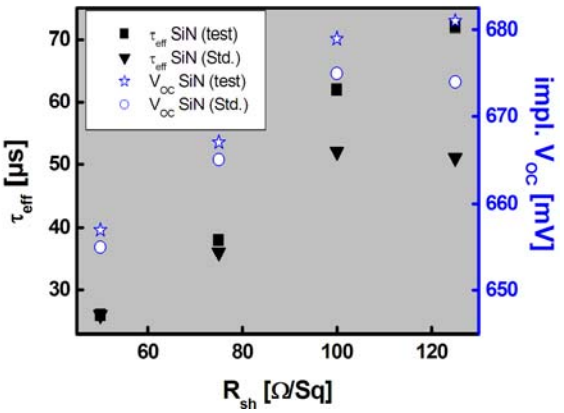

Fig. 6: Measured effective lifetime and implied V_{OC} of samples passivated with different SiN_x-layers and etched emitters with an initial sheet resistance of 50 Ω/Sq. These emitters were etched back to 75, 100 and 120 Ω/Sq.

SUMMARY AND OUTLOOK

We have shown that an etch back emitter can provide both higher open circuit voltages as well as higher short circuit current densities. While some of the gain in short current density will ultimately be lost in the module due to absorption within the glass and lamination foil the gain in open circuit voltage can be completely transferred into the module increasing its efficiency by approximately 0.2%abs.

Based on the presented results we intend to further optimize the devised process in the coming months and apply it to multicrystalline as well as several ribbon silicon materials to determine the overall efficiency gain that can be reached by a selective emitter structure in conjuction with a screen printed metallization on the front side. Furthermore, we will continue working on an improved suitability for large scale production.

ACKNOWLEDGEMENTS

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LITERATURE

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